LISTING OF THE CLAIMS

Please cancel claims 18-22 without prejudice. This Listing of the Claims replaces all previous listings thereof.

1. (Original) A semiconductor memory device comprising an array of memory cells arranged in rows and columns, wherein said array of memory cells comprises:

a plurality of non-intersecting shallow trench isolation (STI) regions isolating a plurality of said columns of memory cells;

a plurality of common source (Vss) lines coupled to a source column arranged according to said columns that are coupled to a plurality of source regions in said array of memory cells; and

an area proximate to a lower portion of non-adjacent said STI regions implanted with n-type dopants for enhancing conductivity of said Vss lines.

2. (Original) The semiconductor memory device as recited in Claim 1 wherein said source column is implanted with n-type dopants isolated between an adjoining pair of said plurality of non-intersecting STI regions.

3. (Original) The semiconductor memory device as recited in Claim 1 wherein said non-adjacent said STI regions comprise alternating said STI regions.

4. (Original) The semiconductor memory device as recited in Claim 3 wherein said n-type dopants for enhancing conductivity of said Vss lines comprise an alternating Vss interconnection.

5. (Original) The semiconductor memory device as described in claim 1, wherein said n-type dopants are selected from the group consisting of antimony and arsenic.

6. (Original) The semiconductor memory device as described in claim 1, wherein said area proximate to a lower portion of non-adjacent said STI regions comprises a region beneath said STI region.

7. (Original) The semiconductor memory device as described in claim 1, wherein diffusion of said n-type dopants for enhancing conductivity of said Vss lines into a substrate further comprising said array does not reach an adjacent said STI region.

8. (Original) The semiconductor memory device as described in claim 1, wherein said n-type dopants for enhancing conductivity of said Vss lines are implanted at low energy.

9. (Original) The semiconductor memory device as described in claim 1, wherein said n-type dopants for enhancing conductivity of said Vss lines are implanted at low dosage.

10. (Original) A non-volatile semiconductor memory device comprising an array of memory cells arranged in rows and columns, wherein said array of memory cells comprises:

a plurality of non-intersecting shallow trench isolation (STI) regions isolating a plurality of said columns of memory cells;

a plurality of common source (Vss) lines coupled to a source column arranged according to said columns that are coupled to a plurality of source regions in said array of memory cells; and

an area proximate to a lower portion of non-adjacent said STI regions implanted with n-type dopants for enhancing conductivity of said Vss lines.

11. (Original) The non-volatile semiconductor memory device as recited in Claim 10 wherein said source column is implanted with n-type dopants isolated between an adjoining pair of said plurality of non-intersecting STI regions.

12. (Original) The non-volatile semiconductor memory device as recited in Claim 10 wherein said non-adjacent said STI regions comprise alternating said STI regions.

13. (Original) The non-volatile semiconductor memory device as recited in Claim 10 wherein said n-type dopants for enhancing conductivity of said Vss lines comprise an alternating Vss interconnection.

14. (Original) The non-volatile semiconductor memory device as described in claim 10, wherein said n-type dopants are taken from a group consisting of antimony and arsenic.

15. (Original) The non-volatile semiconductor memory device as described in claim 10, wherein said area proximate to a lower portion of non-adjacent said STI regions comprises a region beneath said STI region.

16. (Original) The non-volatile semiconductor memory device as described in claim 10, wherein diffusion of said n-type dopants for enhancing conductivity of said Vss lines into a substrate further comprising said array does not reach an adjacent said STI region.

17. (Original) The non-volatile semiconductor memory device as described in claim 10, wherein said n-type dopants for enhancing conductivity of said Vss lines are implanted at low energy and low dosage.

18-22. (Cancelled)